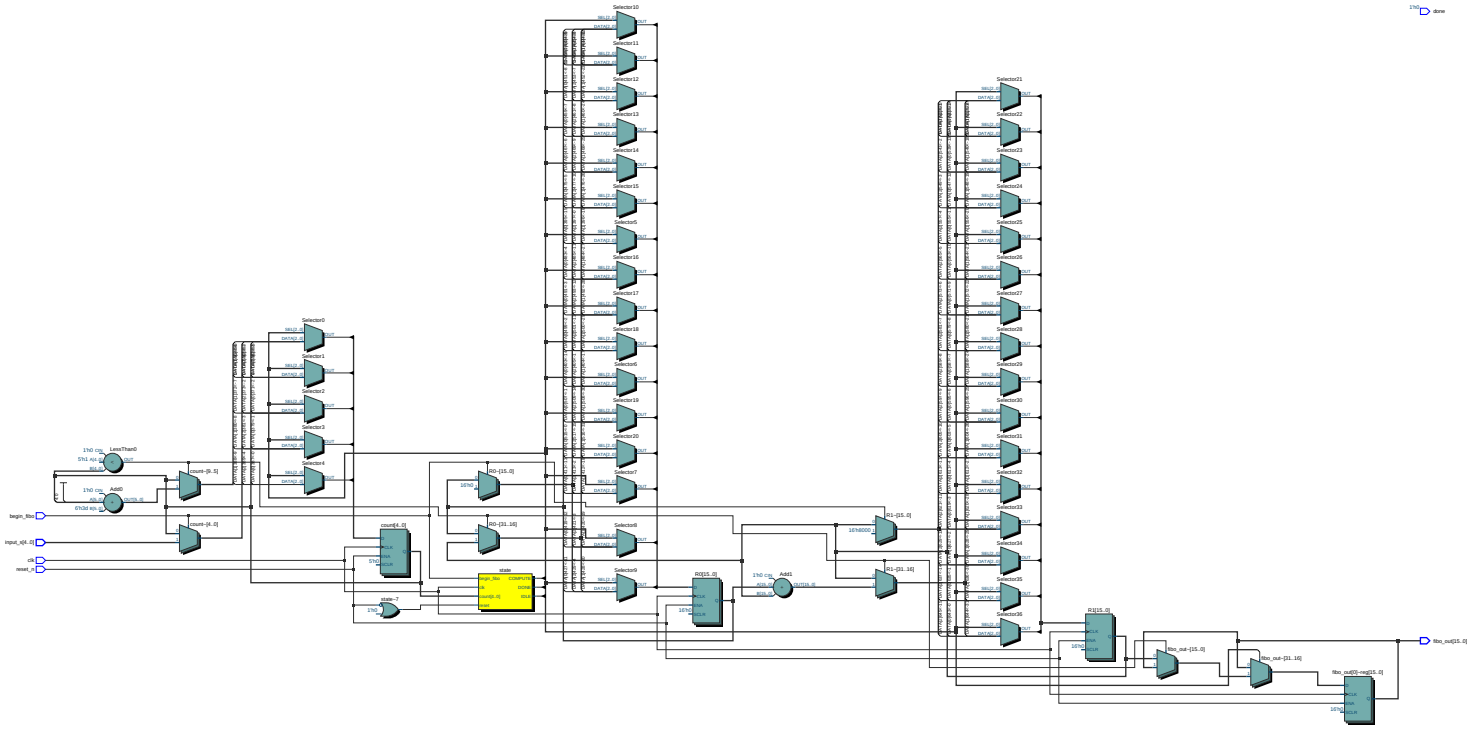
done
begin_fibo
input_x[4..0]
clk
reset_n
LessThan0
Add0
Add1
count-[9..5]
count-[4..0]
count[4..0]
state-7
state
begin_fibo
clk
reset_n
input_x[4..0]
done
R0[15..0]
R1-[15..0]
R0-[31..16]
R1-[31..16]
R1[15..0]
R0[15..0]
fibo_out-[15..0]
fibo_out-[31..16]
fibo_out[0]~reg[15..0]
fibo_out[15..0]